II. REMARKS

Claims 23-32 are pending and stand rejected. Claim 23 has been amended. Attached hereto is Appendix A showing the changes made to Claim 23. Reconsideration is respectfully requested.

1. Drawings

The Final Office Action indicates the drawing corrections submitted on 9/30/02 have been approved. Corrected drawings are now indicated as due. Submitted herewith are formal drawings, which incorporate the approved drawing corrections.

2. Rejection of Claims 23-27 Under § 112

Claims 23-27 were rejected under 35 U.S.C. 112, second paragraph for being indefinite. Specially, the terms "the first insulation layer first portion" and "the first insulation layer second portion" lack proper antecedent basis. Claim 23 has been amended to correct this informality, where these terms now properly recite "the second insulation layer first portion" and "the second insulation layer second portion". The Applicant gratefully appreciates the Examiner's detection of this informality, and respectfully submits no new matter is added and no new search is required.

3. Rejection of Claims 23 and 24 Under § 103(a)

Claims 23-24 were rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,811,853 (Wang), U.S. Patent No. 5,493,138 (Koh) and U.S. Patent 6,091,104 (Chen '104). The applicant respectfully traverses this rejection because A) the combination of references fail to teach the claimed invention, and B) there is no motivation to combine the references relied upon by the Examiner.

A. Wang and Koh combination fail to teach the claimed second insulation layer.

Claim 23 recites a memory device that includes a second insulation layer having a first portion disposed over the first insulation layer and the substrate, a second portion disposed

adjacent the floating gate and a third portion disposed over the floating gate, having a thickness permitting Fowler-Nordheim tunneling of charges therethrough. The Examiner admits on page 3 of the Final Office Action that Wang fails to teach a memory cell having the claimed second insulation layer, but relies on layers 76 and 78 of Koh for teaching such an insulation layer. However, claim 23 an insulation layer with multiple portions, whereas Koh teaches separate insulation layers 76 and 78 (shown as distinct layers of material and formed in separate processing steps, see Col. 5, lines 20-28). Therefore, Koh fails to teach an insulation layer having first, second and third portions as recited in claim 23.

Claim 23 also recites that the control gate has a first portion disposed over the second insulation layer first portion and adjacent to the second insulation layer second portion. Even if the combination of layers 76 and 78 are considered together, there is no portion of control gate 80 of Koh that is both over and adjacent to layers 76/78. Thus, it is respectfully submitted that the combination of references relied upon by the Examiner fails to teach all the elements of claim 23.

B. It is improper to combine Chen with Wang

The Examiner states that it would have been obvious to modify the Wang device with the teaching of Chen '104 (i.e. align the edge of an impurity region with the edge of the vertical sidewall of a gate), to improve the performance of the device (Col. 3, lines 38-40). The Applicant previously argued that such a combination was improper because the references themselves failed provide some teaching whereby the applicant's combination would have been obvious, and it is impermissible simply to engage in a hindsight reconstruction of the claimed invention using the applicant's structure as a template and selecting elements from references to fill the gaps. Interconnect Planning, 774 F.2d at 1143, 227 USPQ at 551. The text cited by the Examiner (Col. 3, lines 38-40) of Chen '104 is merely a general object of the disclosed invention as a whole, with no explicit or implicit reference to the claimed alignment between the gate vertical sidewall and the impurity region, or how that feature would add benefit to other structures.

The Examiner responds on page 6 of the Final Office Action with the conclusion that "In this case, Chen '104 state that to align the edge of an impurity region 64 with the edge of the

vertical sidewall of a gate 59 and a spacer 66 improves the performance of the device. Support for this is given in further detail in Column 5 Line 64 to Column 6 Line 19 and Column 10 Lines 43 to 67 (e.g. faster performance and small sheet size)."

This conclusion is respectfully traversed. The Applicant cannot find any such statement (relating to the alignment of the impurity region 64) in Chen. Moreover, the text cited by the Examiner offers no apparent support for such a statement. Specifically, the cited Column 5/6 text merely discloses the formation of the source drain 63/64 in the substrate, and the doping/size of these regions. The statement about small sheet resistance and better performance relates to the self alignment of the select gate to the floating gate and control gate, not to any alignment of the impurity regions (see Col. 6, lines 14-19). The cited Column 10 text states the small sheet resistance, small loading effect and faster performance result from the particular way the select gate is formed, and again not by any stated alignment to the impurity regions (see Col. 10, lines 57-67). Therefore, it is respectfully submitted that Chen does not provide the requisite motivation for combining the teachings thereof with the device of Wang.

Since the combination of references relied upon by the Examiner fails to teach the claimed invention, and fails to provide a motivation for combining their teachings, the Applicant respectfully submits that claim 23, and claim 24 dependent thereon, are not rendered obvious by Wang, Koh, and Chen '104.

4. Rejection of Claims 25 and 26 Under § 103(a)

Claims 25-26 were rejected under 35 U.S.C. 103(a) as being unpatentable over Wang, Koh, Chen '104, and in further view of admitted Prior Art Figure 1C. Claims 25-26 depend from claim 23, and are therefore considered allowable for the reasons set forth in Part 3 above. The addition of Prior Art Figure 1C does not cure the deficiencies of Wang, Koh, and Chen '104.

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5. Rejection of Claim 27 Under § 103(a)

Claim 27 was rejected under 35 U.S.C. 103(a) as being unpatentable over Wang, Koh, Chen '104, and in further view of U.S. Patent No. 5,751,048 (Lee). Claim 27 depends from claim 23, and is therefore considered allowable for the reasons set forth in Part 3 above. The addition of Lee does not cure the deficiencies of Wang, Koh, and Chen '104.

6. Rejection of Claims 28 and 29 Under § 103(a)

Claims 28-29 were rejected under 35 U.S.C. 103(a) as being unpatentable over Wang, Koh, Chen '104, and in further view of U.S. Patent No. 6,140,182 (Chen '182).

Claim 28 recites the first, second and third portions of the second insulation layer, and specifies the first and second control gate portions in relation to the three second insulation layer portions, in a similar manner as does claim 23. The addition of Chen '182 does not appear to overcome the shortcomings of Wang, Koh, and Chen '104. Therefore, for the reasons set forth in Part 3 above, it is submitted that claim 28, along with claim 29 dependent thereon, are not rendered obvious by these references.

7. Rejection of Claims 30 and 31 Under § 103(a)

Claims 31-32 were rejected under 35 U.S.C. 103(a) as being unpatentable over Wang, Koh, Chen '104, Chen '182, and in further view of admitted Prior Art Figure 1C. Claims 30-31 depend from claim 28, and are therefore considered allowable for the reasons set forth in Part 6 above. The addition of Prior Art Figure 1C does not cure the deficiencies of Wang, Koh, Chen '104 and Chen '182.

8. Rejection of Claim 32 Under § 103(a)

Claim 32 was rejected under 35 U.S.C. 103(a) as being unpatentable over Wang, Koh, Chen '104, Chen '182, and in further view of Lee. Claim 32 depends from claim 28, and is therefore considered allowable for the reasons set forth in Part 6 above. The addition of Lee does not cure the deficiencies of Wang, Koh, Chen '104 and Chen '182.

For the foregoing reasons, it is respectfully submitted that the claims are in an allowable form, and action to that end is respectfully requested.

Respectfully submitted,

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Dated: Jan. 29, 2003 By: _____

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APPENDIX A: MARKINGS TO SHOW CHANGES MADE

23. (Twice Amended) An electrically programmable and erasable memory device comprising:

a substrate of semiconductor material of a first conductivity type;

first and second spaced-apart regions in the substrate of a second conductivity type, with a channel region therebetween;

a first insulation layer disposed over said substrate;

an electrically conductive floating gate disposed over said first insulation layer and extending over a portion of the channel region and over a portion of the first region;

a second insulation layer having a first portion disposed over said first insulation layer and said substrate, a second portion disposed adjacent the floating gate and a third portion disposed over the floating gate, wherein the second insulation layer has a thickness permitting Fowler-Nordheim tunneling of charges therethrough;

an electrically conductive control gate having a first portion disposed over the [first] second insulation layer first portion and adjacent to the [first] second insulation layer second portion, and a second portion extending over the second insulation layer third portion, the control gate having a substantially vertical sidewall portion; and

an insulation spacer formed adjacent to the substantially vertical sidewall portion of the control gate;

wherein the second region has an edge that is aligned with the substantially vertical sidewall portion.